AMENDMENTS TO CLAIMS

This listing of claims will replace all prior versions and listings of claims in this application.

Listing of Claims

1-8. (Cancelled).

9. (Previously presented) A method for fabricating a semiconductor component having a stress-absorbing semiconductor layer, comprising the steps of:

a) forming a carrier material having a first lattice constant;

b) forming a crystalline stress generator layer having in its final atom layer substantially a second lattice constant being different from the first lattice constant on the carrier material in order to generate a mechanical stress;

c) forming an insulating stress transmission layer having a third lattice constant being matched to first lattice constant of the carrier material on the stress generator layer for transmitting the mechanical stress that has been generated;

d) forming a crystalline, stress-absorbing semiconductor layer having a lattice constant different from the second lattice constant, which is different than the first lattice constant, on the stress transmission layer for the purpose of absorbing the mechanical stress;

e) forming a gate dielectric on the stress-absorbing semiconductor layer;

f) forming a control layer on the gate dielectric;

g) patterning the gate dielectric and the control layer; and

h) forming source/drain regions in the stress-absorbing semiconductor layer.

10. (Previously presented) The method as recited in claim 9, wherein in step a) a semiconductor substrate having a (100) surface orientation is provided, and a semiconductor buffer layer is epitaxially deposited thereon in order to produce a smooth surface.

11. (Previously presented) The method as recited in claim 9, wherein in step b) a IV-IV or III-V semiconductor is used.

12. (Previously presented) The method as recited in claim 11, wherein in step b) a multiple layer sequence is formed as the stress generator layer.

13. (Previously presented) The method as recited in claim 9, wherein in step b) the stress generator layer is smoothed by means of a molecular beam epitaxy process.

14. (Previously presented) The method as recited in claim 9, wherein in step c) a crystalline insulator layer is formed as the stress transmission layer.

15. (Previously presented) The method as recited in claim 14, wherein in step c) the stress transmission layer with a lattice constant which is matched to the second lattice constant of the stress-absorbing semiconductor layer is formed.

16. (Previously presented) The method as recited in claim 15, wherein in step c) only a few atom layers of the stress transmission layer are deposited epitaxially on the stress generator layer.

17. (Previously presented) The method as recited in claim 9, wherein in step d) a fully depleted semiconductor material is used.

18. (Previously presented) The method as recited in claim 9, wherein in step e) a material with a high dielectric constant is used as the gate dielectric.

19. (Previously presented) The method as recited in claim 9, wherein in step f) a metal is used as the control layer.

20. (Previously presented) The method as recited in claim 9, wherein

in step a) Si is used as the carrier material;

in step b) SiGe is used as the stress generator layer;

in step c) CaF_2 is used as the stress transmission layer;

in step d) Si is used as the stress-absorbing semiconductor layer;

in step e) HfO_2 is used as the gate dielectric; and

in step f) TiN is used as the control layer.

21. (Previously presented) The method recited in claim 9 further comprising defining a channel between the source/drain regions, the channel having a channel length L, wherein the stress-absorbing region has a thickness d which is less than one-third the channel length L.

22. (Currently amended) A method for fabricating a semiconductor component, the method comprising the steps of:

a) forming a crystalline carrier material having a first lattice constant;

b) forming a crystalline stress generator layer having in its final atom layer substantially a second lattice constant being different from the first lattice constant on the carrier material in order to generate a mechanical stress;

c) forming an insulating stress transmission layer having a third lattice constant being matched to the first lattice constant of the carrier material on the stress generator layer for transmitting the mechanical stress that has been generated, the stress transmission layer having a stress transmission lattice constant; and

d) forming a crystalline, stress-absorbing semiconductor layer on the stress transmission layer for the purpose of absorbing the mechanical stress transmitted by the stress transmission layer, the stress-absorbing semiconductor layer having a lattice constant different from the second lattice constant, which is different from the first lattice constant and which substantially matches the third [[a]] lattice constant of the stress transmission layer for transmitting stress from the stress transmission layer to the stress-absorbing layer.

23. (Previously presented) The method recited in claim 22 further comprising

e) forming a gate dielectric on the stress-absorbing semiconductor layer;

f) forming a control layer on the gate dielectric;

g) patterning the gate dielectric and the control layer; and

h) forming source/drain regions in the stress-absorbing semiconductor layer.

24. (Previously presented) The method as recited in claim 22, wherein

in step a) Si is used as the carrier material;

in step b) SiGe is used as the stress generator layer;

in step c) CaF_2 is used as the stress transmission layer; and

in step d) Si is used as the stress-absorbing semiconductor layer.

25. (Previously presented) The method recited in claim 23 further comprising defining a channel between the source/drain regions, the channel having a channel length L, wherein the stress-absorbing region has a thickness d which is less than one-third the channel length L.

26. (Currently amended) A method for fabricating a semiconductor component, the method comprising the steps of:

a) forming a crystalline carrier material having a carrier lattice constant;

b) forming a stress generator layer on the crystalline carrier material, the stress generator layer selected to have in its final atom layer a first lattice constant which is ~~slightly~~ different from the carrier lattice constant to generate mechanical stress;

c) forming an insulating crystalline stress transmission layer on the stress generator layer, the insulating crystalline stress transmission layer selected to have a transmission layer lattice constant which is matched ~~very similar~~ to the first lattice constant of the stress generator layer to enhance transmission of the mechanical stress generated in the stress generator layer to a following layer; and

d) forming a stress absorbing layer on the stress transmission layer, the stress absorbing layer having a second lattice constant, which is different than the first lattice constant, which is different than the carrier lattice constant, the second lattice constant selected to enhance transmission of the mechanical stress from the stress transmission layer to the stress absorbing layer to improve charge carrier mobility in the stress absorbing layer and to improve selected electrical properties of the semiconductor component.

27. (Previously presented) The method of claim 26 further comprising:

defining an active region in the stress absorbing layer, the active region having a thickness d; and

forming a field effect transistor as the semiconductor component in the active region, the field effect transistor having a channel length L such that the thickness d is less than one-third the channel length L.

28. (Previously presented) The method recited in claim 27 wherein forming a field effect transistor comprises:

e) forming a gate dielectric on the stress-absorbing semiconductor layer;

f) forming a control layer on the gate dielectric;

g) patterning the gate dielectric and the control layer to define the channel length L; and

h) forming source/drain regions in the stress-absorbing semiconductor layer.